IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Snyder, et al.

Serial No. : _____ Examiner: _____

Filed : _____ Group Art Unit: _____

For : PROGRAMMABLE MICROCONTROLLER ARCHITECTURE (MIXED ANALOG/DIGITAL)

A continuation of: PROGRAMMABLE MICROCONTROLLER ARCHITECTURE (MIXED ANALOG/DIGITAL), by Snyder, et al., Serial No. 09/924,734, filed 08/07/01.

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents & Trademarks
Washington, D.C. 20231

Sir:

Please enter the following preliminary amendments to the claims:

IN THE CLAIMS

Please cancel Claims 1-23.

Please add the following new Claims:

24. (new) A circuit comprising:

a plurality of analog circuit blocks;

a plurality of digital circuit blocks;

a bus coupling analog input/output data and digital input/output data for the plurality of analog circuit blocks and the plurality of digital circuit blocks; and

a system clock for controlling the coupling of the analog input/output data and the digital input output data to the bus.

25. (new) A circuit according to Claim 24 further comprising:

a programmable interconnect structure coupled to the plurality of analog circuit blocks and the plurality of digital circuit blocks.

26. (new) A circuit according to Claim 25 wherein the programmable interconnect structure is configured to dynamically reconfigure the plurality of analog circuit blocks and the plurality of digital circuit blocks to implement one of a plurality of functions.

27. (new) A circuit according to Claim 24 wherein the circuit comprises a single integrated circuit semiconductor chip.

28. (new) A circuit according to Claim 24 wherein the analog circuit blocks comprises at least one continuous time analog circuit.

29. (new) A circuit according to Claim 24 wherein the analog circuit blocks comprises at least one switched capacitor analog circuit.

30. (new) A microcontroller comprising:

a plurality of programmable analog circuit blocks;

a plurality of programmable digital circuit blocks;

a programmable interconnect coupling the analog circuit blocks and the digital circuit blocks;

a bus coupling analog input/output data and digital input/output data for the analog circuit blocks and the digital circuit blocks; and

a system clock for controlling the bus.

31. (new) A microcontroller according to Claim 30 wherein one of the digital circuit blocks is configured to implement logical operations.

32. (new) A microcontroller according to Claim 30 wherein one of the digital circuit blocks is configured to implement computational operations.

33. (new) A microcontroller according to Claim 30 wherein the programmable interconnect structure and the programmable analog circuit blocks and the plurality of programmable digital circuit blocks are constructed on a semiconductor chip.

34. (new) A microcontroller according to Claim 30 wherein the programmable analog circuit blocks comprise at least one continuous time analog circuit block.

35. (new) A microcontroller according to Claim 30 wherein the programmable analog circuit blocks comprise at least one switched capacitor analog circuit block.

36. (original) A microcontroller according to Claim 30 wherein the programmable digital circuit blocks comprise at least one digital multi-function circuit block having a first set of digital functions and at least one digital multi- function circuit block having a second set of digital functions different from the first set.

37. (new) A method of providing a dynamically programmable analog/digital communication interface circuit, comprising:

configuring a plurality of programmable analog circuit blocks to implement at least one of a plurality of analog functions,

configuring a plurality of programmable digital circuit blocks to implement at least one of a plurality of digital functions,

configuring a routing matrix to couple analog data and digital data between the programmable analog circuit blocks and the programmable digital circuit blocks; and

transferring data via a bus independent of the routing matrix and in accordance with at least one system clock.

38. (new) The method according to Claim 37 wherein flash memory is used to program the routing matrix and the plurality of programmable analog circuit blocks and the plurality of programmable digital circuit blocks and to enable dynamic circuit reconfiguration.

39. (new) The method according to Claim 37 wherein the programmable analog circuit blocks comprise at least one continuous time analog circuit and at least one switched capacitor analog circuit.

40. (new) The method according to Claim 37 wherein the programmable digital circuit blocks comprise at least one standard digital multi-function circuit having a first set

of digital functions and at least one enhanced digital multi- function circuit having at least one function differing from the first set of digital functions.

41. (new) The method according to Claim 37 wherein the programmable analog circuit blocks comprise at least one multi-function circuit programmable for at least one of the plurality of analog functions and at least one fixed function circuit programmable for a fixed function with at least one of a number of different parameters.

42. (new) The method according to Claim 37 wherein the plurality of digital functions comprises logical operations.

43. (new) The method according to Claim 37 wherein the plurality of digital functions comprises computational operations.

Respectfully submitted,
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